

LM5030 100V Push-Pull Current Mode PWM Controller

Check for Samples: [LM5030](#)

FEATURES

- Internal High Voltage Start-up Regulator
- Single Resistor Oscillator Setting
- Synchronizable
- Error Amplifier
- Precision Reference
- Adjustable Softstart
- Dual Mode Over-Current Protection
- Slope Compensation
- Direct Optocoupler Interface
- 1.5A Peak Gate Drivers
- Thermal Shutdown

PACKAGES

- VSSOP-10
- Thermally Enhanced WSON-10 (4mm x 4mm).

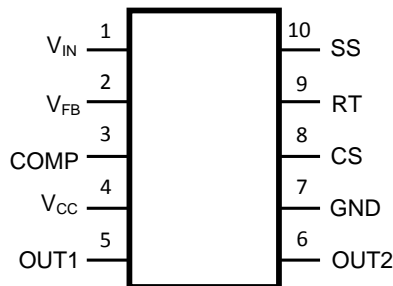
APPLICATIONS

- Telecommunication Power Converters
- Industrial Power Converters
- +42V Automotive Systems

DESCRIPTION

The LM5030 High Voltage PWM controller contains all of the features needed to implement Push-Pull and Bridge topologies, using current-mode control in a small 10 pin package. This device provides two alternating gate driver outputs. The LM5030 includes a high-voltage start-up regulator that operates over a wide input range of 14V to 100V. Additional features include: error amplifier, precision reference, dual mode current limit, slope compensation, softstart, sync capability and thermal shutdown. This high speed IC has total propagation delays less than 100ns and a 1MHz capable single resistor adjustable oscillator.

Connection Diagram



**Figure 1. Top View
10-Lead VSSOP, WSON**



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Block Diagram

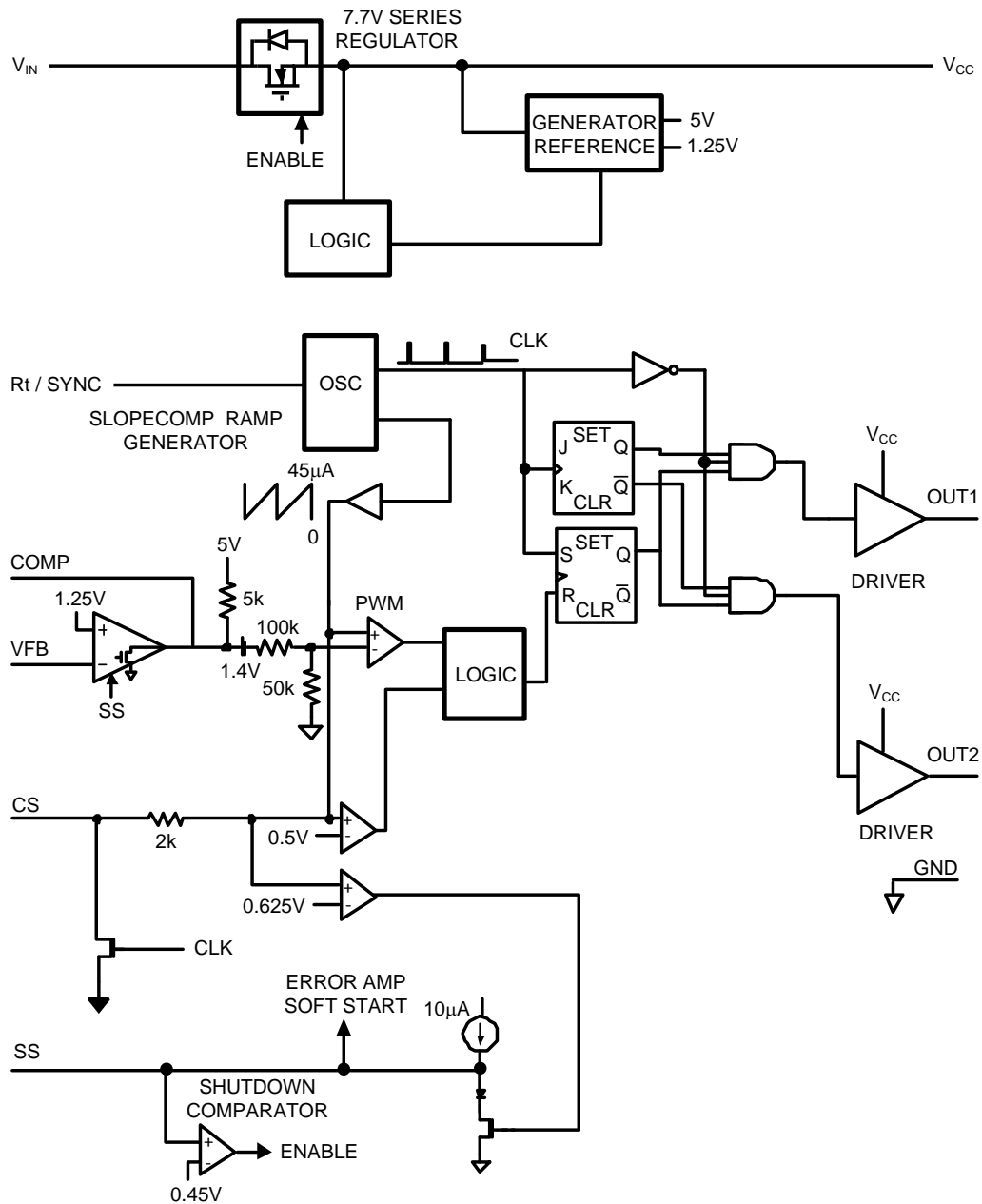


Figure 2.

PIN DESCRIPTION

Pin Name	Pin Number	Description	Application Information
V _{IN}	1	Source Input Voltage	Input to start-up regulator. Input range 14 to 100 Volts.
V _{FB}	2	Inverting input to the error amplifier	The non-inverting input is internally connected to a 1.25 Volt reference.
COMP	3	Output to the error amplifier	There is an internal 5K resistor pull-up on this pin. The error amplifier provides an active sink.
V _{CC}	4	Output from the internal high voltage series pass regulator. The regulation setpoint is 7.7 Volts.	If an auxiliary winding raises the voltage on this pin above the regulation setpoint the internal series pass regulator will shutdown, reducing the IC power dissipation.
OUT1	5	Output of the PWM controller	Alternating PWM output gate driver.
OUT2	6	Output of the PWM controller	Alternating PWM output gate driver.
GND	7	Return	Ground
CS	8	Current sense input	Current sense input for current mode control and current limit sensing. Using separate dedicated comparators, if CS exceeds 0.5 Volt the outputs will go into Cycle by Cycle current limit. If CS exceeds 0.625V the outputs will be disabled and a softstart commenced.
RT	9	Oscillator timing resistor pin and synchronization input.	An external resistor sets the oscillator frequency. This pin will also accept synchronization pulses from an external oscillator.
SS	10	Dual purpose Softstart and Shutdown pin	A 10μA current source and an external capacitor set the softstart timing length. The controller will enter a low power state if the SS pin is pulled below the typical shutdown threshold of 0.45V.
WSON DAP	SUB	Die Substrate	The exposed die attach pad on the WSON package should be connected to a PCB thermal pad at ground potential. For additional information on using TI's No Pull Back WSON package, please refer to WSON Application Note AN-1187.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

V_{IN} to GND (Survival)		-0.3V to 100V
V_{CC} to GND (Survival)		-0.3V to 16V
RT to GND (Survival)		-0.3V to 5.5V
All other pins to GND (Survival)		-0.3V to 7V
Power Dissipation		Internally Limited
ESD Rating ⁽³⁾	Human Body Model	2kV
	Machine Model	200V
Lead Temperature (Soldering 4 seconds)		260°C
Storage Temperature Range		-55°C to +150°C
Junction Temperature		150°C

- (1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin. The machine model ESD rating for pin 5 and pin 6 is 150V.

Operating Ratings

Junction Temperature	-40°C to +105°C
V_{IN}	14V to 90V

Electrical Characteristics

Specifications in standard type face are for $T_J = +25^\circ\text{C}$ and those in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified: $V_{IN} = 48\text{V}$, $V_{CC} = 10\text{V}$, and $R_T = 26.7\text{k}\Omega$

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
Startup Regulator						
V_{CCReg}	V_{CC} Regulation	open ckt	7.4	7.7	8.0	V
	V_{CC} Current Limit	See	10	17		mA
$I-V_{IN}$	Startup Regulator Leakage (external V_{CC} Supply)	$V_{IN} = 90\text{V}$		150	500	μA
I_{IN}	Shutdown Current	$SS = 0\text{V}$, $V_{CC} = \text{open}$		250	350	μA
V_{CC} Supply						
	V_{CC} undervoltage Lockout Voltage		VccReg - 300mV	VccReg - 100mV		V
	Undervoltage Hysteresis		1.2	1.6	2.1	V
I_{CC}	Supply Current	$C_{load} = 0$		2	3	mA

- (1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
- (2) Typical numbers represent the most likely parametric norm for 25°C operation.

Electrical Characteristics (continued)

Specifications in standard type face are for $T_J = +25^\circ\text{C}$ and those in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified: $V_{IN} = 48\text{V}$, $V_{CC} = 10\text{V}$, and $R_T = 26.7\text{k}\Omega$

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
Error Amplifier						
GBW	Gain Bandwidth			4		MHz
	DC Gain			75		dB
	Input Voltage	$V_{FB} = \text{COMP}$	1.220	1.245	1.270	V
	COMP Sink Capability	$V_{FB} = 1.5\text{V}$ COMP= 1V	5	13		mA
Current Limit						
CS1	Cycle by Cycle CS Threshold Voltage		0.45	0.5	0.55	V
CS2	Restart CS Threshold Voltage	Resets SS capacitor; auto restart	0.575	0.625	0.675	V
	ILIM Delay to Output	CS step from 0 to 0.6V Time to onset of OUT Transition (90%) Load = 0		30		ns
	CS Sink Current (clocked)	CS = 0.3V	3	6		mA
Soft Start/Shutdown						
	Softstart Current Source		7	10	13	μA
	Softstart to COMP Offset		0.25	0.5	0.75	V
	Shutdown Threshold		0.2	0.45	0.7	V
Oscillator						
	Frequency1 (RT = 26.7K)		175	200	225	kHz
	Frequency2 (RT = 8.2K)		510	600	690	kHz
	Sync threshold			3.2	3.8	V
PWM Comparator						
	Delay to Output	COMP set to 2V CS stepped 0 to 0.4V, Time to onset of OUT transition low		30		ns
	Max Duty Cycle	Inferred from deadtime	47.5	49	50	%
	Min Duty Cycle	COMP=0V			0	%
	COMP to PWM Comparator Gain			0.34		
	COMP Open Circuit Voltage	$V_{FB} = 0\text{V}$	4.3	5.2	6.1	V
	COMP Short Circuit Current	$V_{FB} = 0\text{V}$, COMP=0V	0.6	1.1	1.5	mA
Slope Compensation						
	Slope Comp Amplitude	Delta increase at PWM Comparator to CS	80	105	130	mV
Output Section						
	Deadtime	Load = 0, 10% to 10%	85	135	185	ns
	Output High Saturation	$I_{OUT} = 50\text{mA}$, $V_{CC} - V_{OUT}$		0.25	0.75	V
	Output Low Saturation	$I_{OUT} = 100\text{mA}$		0.25	0.75	V
	Rise Time	Load = 1nF		16		ns
	Fall Time	Load = 1nF		16		ns
Thermal Shutdown						
Tsd	Thermal Shutdown Temp.			165		$^\circ\text{C}$
	Thermal Shutdown Hysteresis			15		$^\circ\text{C}$

Typical Performance Characteristics

Unless otherwise specified: $T_J = 25^\circ\text{C}$.

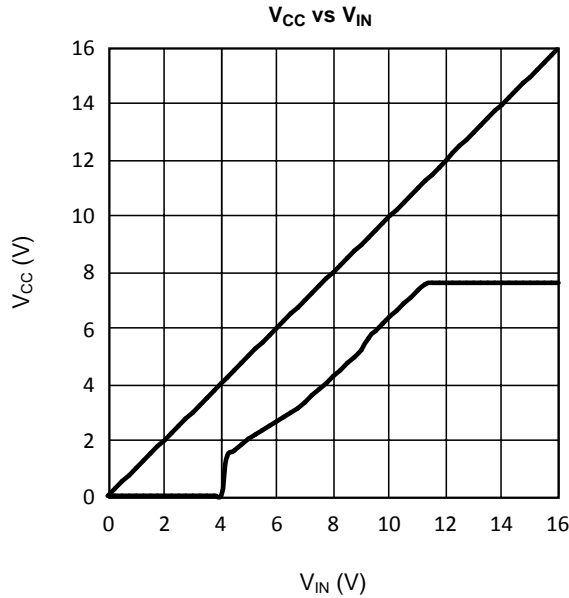


Figure 3.

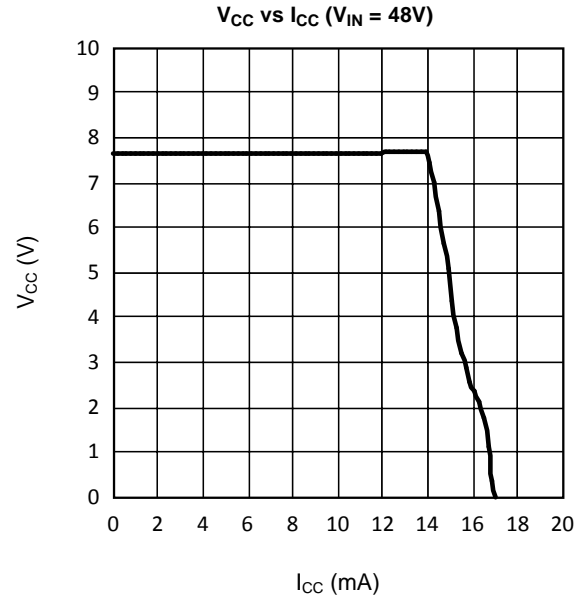


Figure 4.

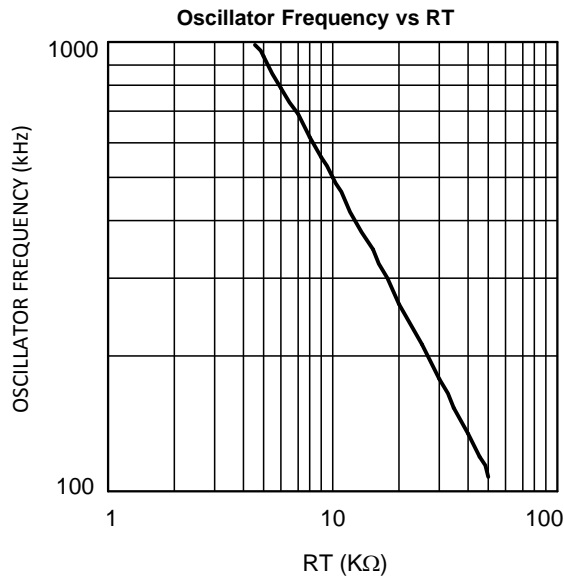


Figure 5.

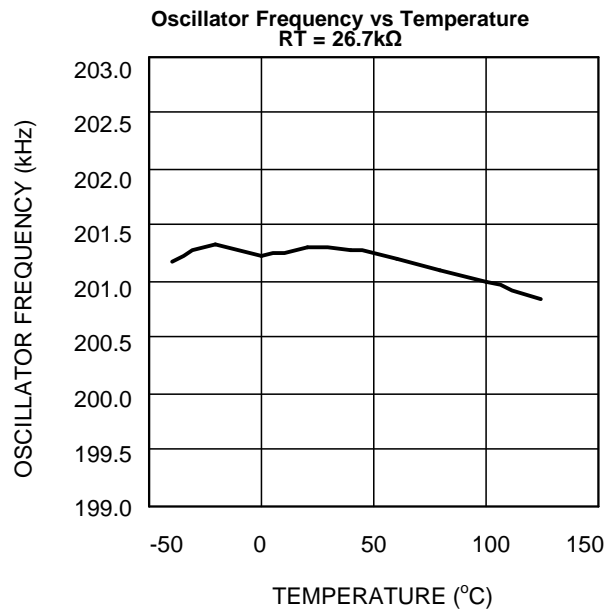


Figure 6.

Typical Performance Characteristics (continued)

Unless otherwise specified: $T_J = 25^\circ\text{C}$.

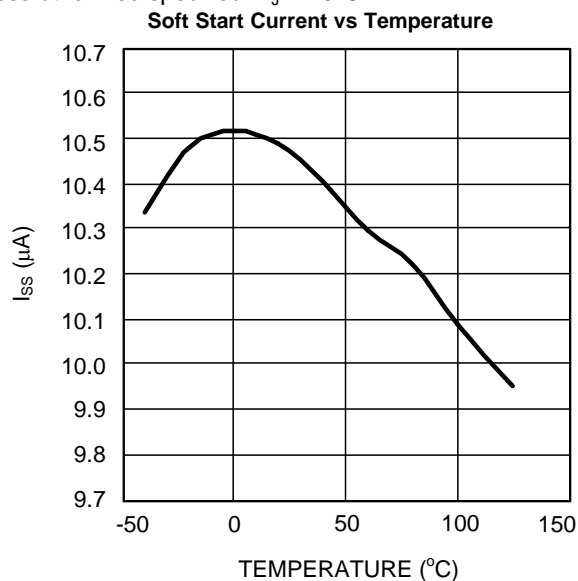


Figure 7.

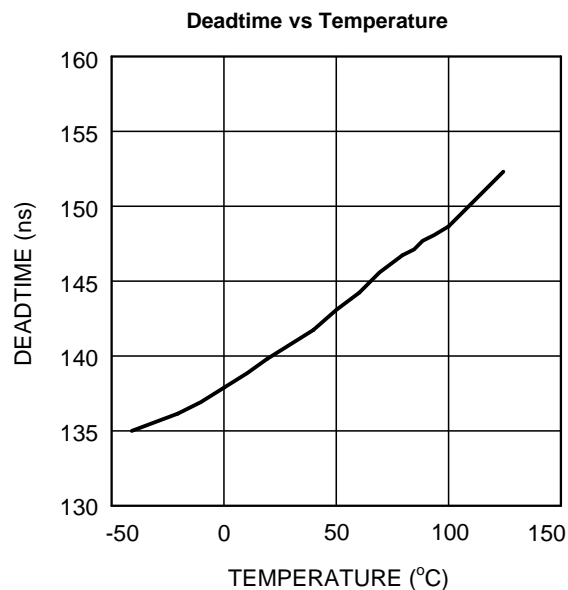


Figure 8.

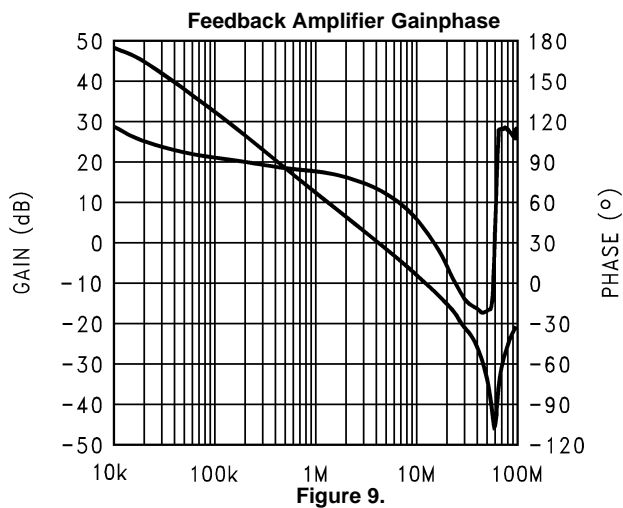


Figure 9.

DETAILED OPERATING DESCRIPTION

The LM5030 High Voltage PWM controller contains all of the features needed to implement Push-Pull and Bridge topologies, using current-mode control in a small 10 pin package. Features included are, startup regulator, dual mode current limit, dual alternating gate drivers, thermal shutdown, softstart and slope compensation. This high speed IC has total propagation delays <100nS. The Functional Block Diagram of the LM5030 is shown in [Figure 2](#).

The LM5030 is designed for Current-Mode Control converters which require alternating outputs, such as Push-Pull and Half/Full Bridge topologies. The features included in the LM5030 enable all of the advantages of Current-Mode Control, line feed-forward, cycle by cycle current limit and simplified loop compensation. The oscillator ramp is internally buffered and added to the PWM comparator input to provide slope compensation necessary for current mode control at higher duty cycles.

High Voltage Start-Up Regulator

The LM5030 contains an internal high voltage startup regulator. The input pin (V_{in}) can be connected directly to line voltages as high as 100V. The regulator output is internally current limited to 10mA. Upon power up, the regulator is enabled and sources current into an external capacitor connected to the V_{CC} pin. The recommended capacitance range for the V_{CC} regulator is 0.1 μ F to 50 μ F. When the voltage on the V_{CC} pin reaches the regulation point of 7.7V, the controller outputs are enabled. The outputs will remain enabled unless, V_{CC} falls below 6.1V or if the SS/SHUTDOWN pin is pulled to ground or an over temperature condition occurs. In typical applications, an auxiliary transformer winding is diode connected to the V_{CC} pin. This winding raises the V_{CC} voltage greater than 8V, effectively shutting off the internal startup regulator and saving power while reducing the controller dissipation. The external V_{CC} capacitor must be sized such that the self-bias will maintain a V_{CC} voltage greater than 6.1V during the initial start-up. During a fault mode when the converter self bias winding is inactive, external current draw on the V_{CC} line should be limited as to not exceed the maximum power dissipation of the controller. An external start-up or other bias rail can be used instead of the internal start-up regulator by connecting the V_{CC} and the V_{in} pins and feeding the external bias voltage (8 - 15V) to that node.

Error Amplifier

An internal high gain error amplifier is provided within the LM5030. The amplifier's non-inverting reference is tied to 1.25V. In non-isolated applications the power converter output is connected to the VFB pin via the voltage setting resistors and loop compensation is connected between the COMP and VFB pins.

For most isolated applications the error amplifier function is implemented on the secondary side ground. Since the internal error amplifier is configured as an open drain output it can be disabled by connecting VFB to ground. The internal 5K pull-up resistor, connected between the 5V reference and COMP, can be used as the pull-up for an optocoupler or other isolation device.

PWM Comparator

The PWM comparator compares the compensated current ramp signal to the loop error voltage from the internal error amplifier (COMP pin). This comparator is optimized for speed in order to achieve minimum discernable duty cycles. The comparator polarity is such that zero Volts on the COMP pin will cause a zero duty cycle.

Current Limit/ Current Sense

The LM5030 contains two levels of over-current protection. If the voltage on the current sense comparator exceeds 0.5 Volts the present cycle is terminated (cycle by cycle current limit). If the voltage on the current sense comparator exceeds 0.625 Volts, the controller will terminate the present cycle and discharge the softstart capacitor. A small RC filter, located near the controller, is recommended for the CS pin. An internal MOSFET discharges the current sense filter capacitor at the conclusion of every cycle, to improve dynamic performance.

The LM5030 CS and PWM comparators are very fast, and as such will respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the pins of the IC (CS and RTN). Also if a current sense transformer is used, both leads of the transformer secondary should be routed to the sense resistor, which should also be located close to the IC. If a current sense resistor located in the drive transistor sources is used, for current sense, a low inductance resistor should be chosen. In this case all of the noise sensitive low power grounds should be commoned together around the IC and then a single connection should be made to the power ground (sense resistor ground point).

The second level threshold is intended to protect the power converter by initiating a low duty cycle hiccup mode when abnormally high, fast rising currents occur. During excessive loading, the first level threshold will always be reached and the output characteristic of the converter will be that of a current source but this sustained current level can cause excessive temperatures in the power train especially the output rectifiers. If the second level threshold is reached, the softstart capacitor will be fully discharged, a retry will commence following the discharge detection. The second level threshold will only be reached when a high dV/dt is present at the current sense pin. The signal must be fast enough to reach the second level threshold before the first threshold detector turns off the driver. This can usually happen for a saturated power inductor or shorted load. Excessive filtering on the CS pin, extremely low value current sense resistor or an inductor that does not saturate with excessive loading may prevent the second level threshold from ever being reached.

Oscillator, Shutdown and Sync Capability

The LM5030 oscillator is set by a single external resistor connected between the RT pin and return. To set a desired oscillator frequency the necessary RT resistor can be calculated as:

$$RT = \frac{(1/F) - 172 \times 10^{-9}}{182 \times 10^{-12}} \quad (1)$$

Each output switches at half the oscillator frequency in a Push-Pull configuration. The LM5030 can also be synchronized to an external clock. The external clock must be of higher frequency than the free running frequency set by the RT resistor. The clock signal should be capacitively coupled into the RT pin with a 100pF capacitor. A peak voltage level greater than 3 Volts with respect to ground is required for detection of the sync pulse. The sync pulse width should be set in the 15 to 150nS range by the external components. The RT resistor is always required, whether the oscillator is free running or externally synchronized. The voltage at the RT pin is internally regulated to a nominal 2 Volts.

The RT resistor should be located very close to the device and connected directly to the pins of the IC (RT and GND).

Slope Compensation

The PWM comparator compares the current sense signal to the voltage derived from the COMP pin. The COMP voltage is set by either the internal error amplifier or an external error amplifier through an optocoupler. At duty cycles greater than 50% (composite of alternating outputs) current mode control circuits are prone to subharmonic oscillation. By adding an additional ramp signal to the current sense ramp signal this condition can be avoided. The LM5030 integrates this slope compensation by buffering the internal oscillator ramp and summing it internally to the current sense (CS) signal. Additional slope compensation may be added by increasing the source impedance of the current sense signal.

Soft Start/ Shutdown

The softstart feature allows the converter to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. An internal 10uA current source and an external capacitor generate a ramping voltage signal which limits the error amplifier output during start-up. In the event of a second level current limit fault, the softstart capacitor will be fully discharged which disables the output drivers. When the fault condition is no longer present, the softstart capacitor is released to ramp and gradually restart the converter. The SS pin can also be used to disable the controller. If the SS pin voltage is pulled down below 0.45V (nominal) the controller will disable the outputs and enter a low power state.

OUT1, OUT2 and Time Delay

The LM5030 provides two alternating outputs, OUT1 and OUT2. The internal gate drivers can each sink 1.5A peak each. The maximum duty cycle for each output is inherently limited to less than 50%. The typical deadtime between the falling edge of one gate driver output and the rising edge of the other gate driver output is 135ns.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the excessive junction temperature. When activated, typically at 165 degrees Celsius, the controller is forced into a low power reset state, disabling the output drivers and the bias regulator. This feature is provided to prevent catastrophic failures from accidental device overheating.

Typical Application Circuit

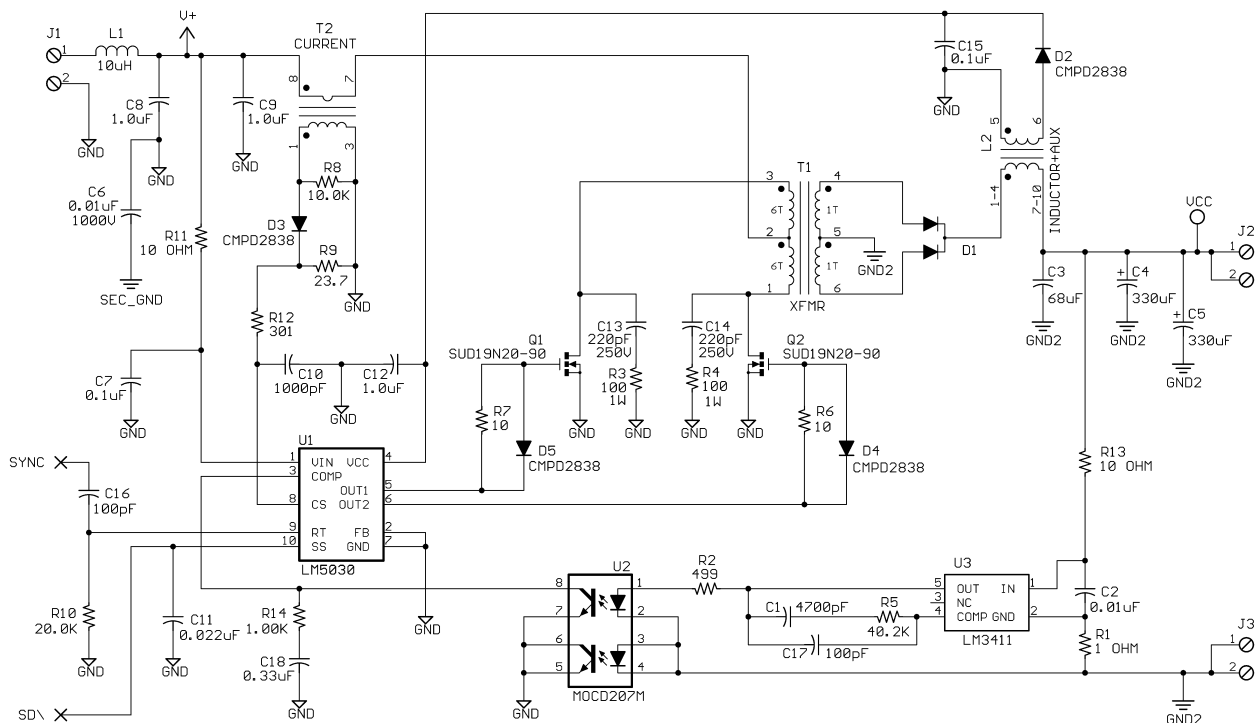




Figure 10. Typical Application Circuit, 36V - 75VIN and 3.3V, 10A OUT

ITEM		PART NUMBER	DESCRIPTION	VALUE
C	1	C0805C472K5RAC	Capacitor, CER, KEMET	4700p, 50V
C	2	C0805C103K5RAC	Capacitor, CER, KEMET	0.01μ, 50V
C	3	C4532X7S0G686M	Capacitor, CER, TDK	68μ, 4V
C	4	T520D337M006AS4350	Capacitor, TANT, KEMET	330μ, 6.3V
C	5	T520D337M006AS4350	Capacitor, TANT, KEMET	330μ, 6.3V
C	6	C4532X7R3A103K	Capacitor, CER, TDK	0.01μ, 1000V
C	7	C3216X7R2A104K	Capacitor, CER, TDK	0.1μ, 100V
C	8	C4532X7R2A105M	Capacitor, CER, TDK	1μ, 100V
C	9	C4532X7R2A105M	Capacitor, CER, TDK	1μ, 100V
C	10	C0805C102K1RAC	Capacitor, CER, KEMET	1000p, 100V
C	11	C1206C223K5RAC	Capacitor, CER, KEMET	0.022μ, 50V
C	12	C3216X7R1E105M	Capacitor, CER, TDK	1μ, 25V
C	13	C3216COG2J221J	Capacitor, CER, TDK	220p, 630V
C	14	C3216COG2J221J	Capacitor, CER, TDK	220p, 630V
C	15	C1206C104K5RAC	Capacitor, CER, KEMET	0.1μ, 50V
C	16	C0805C101J1GAC	Capacitor, CER, KEMET	100p, 100V
C	17	C0805C101J1GAC	Capacitor, CER, KEMET	100p, 100V
C	18	C3216X7R1H334K	Capacitor, CER, TDK	0.33μ, 50μ
D	1	MBRB3030CTL	Diode, Schottky, ON	
D	2	CMPD2838-NSA	Diode, Signal, Central	
D	3	CMPD2838-NSA	Diode, Signal, Central	
D	4	CMPD2838-NSA	Diode, Signal, Central	
D	5	CMPD2838-NSA	Diode, Signal, Central	
L	1	MSS6132-103	Input Choke, Coilcraft	10μH, 1.5A
L	2	A9785-B	Output Choke, Coilcraft	7μH
R	1	CRCW12061R00F	Resistor	1
R	2	CRCW12064990F	Resistor	499
R	3	CRCW2512101J	Resistor	100, 1W
R	4	CRCW2512101J	Resistor	100, 1W
R	5	CRCW12064022F	Resistor	40.2K
R	6	CRCW120610R0F	Resistor	10
R	7	CRCW120610R0F	Resistor	10
R	8	CRCW12061002F	Resistor	10K
R	9	CRCW120623R7F	Resistor	23.7
R	10	CRCW12062002F	Resistor	20K
R	11	CRCW120610R0F	Resistor	10
R	12	CRCW12063010F	Resistor	301
R	13	CRCW120610R0F	Resistor	10
R	14	CRCW12061001F	Resistor	1K
TX	1	A9784-B	POWER XFR, COILCRAFT	
TX	2	P8208T	CURRENT XFR, Pulse	100:1
U1	1	LM5030	REGULATOR, TI	
U2	2	MOCD207M	OPTO-COUPLER, QT OPTOELECTRONICS	
U3	3	LM3411AM5-3.3	REFERENCE, TI	
		651-1727010	DUAL TERMINALS, MOUSER	3 per ASSY
X	1	SUD19N20-90	FET, N, 200V, SILICONIX	
X	2	SUD19N20-90	FET, N, 200V, SILICONIX	

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5030MM	NRND	VSSOP	DGS	10	1000	TBD	Call TI	Call TI	-40 to 125	S73B	
LM5030MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S73B	
LM5030MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S73B	
LM5030SD/NOPB	ACTIVE	WSO	DPR	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5030SD	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5030MM	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5030MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5030MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5030SD/NOPB	WSOP	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

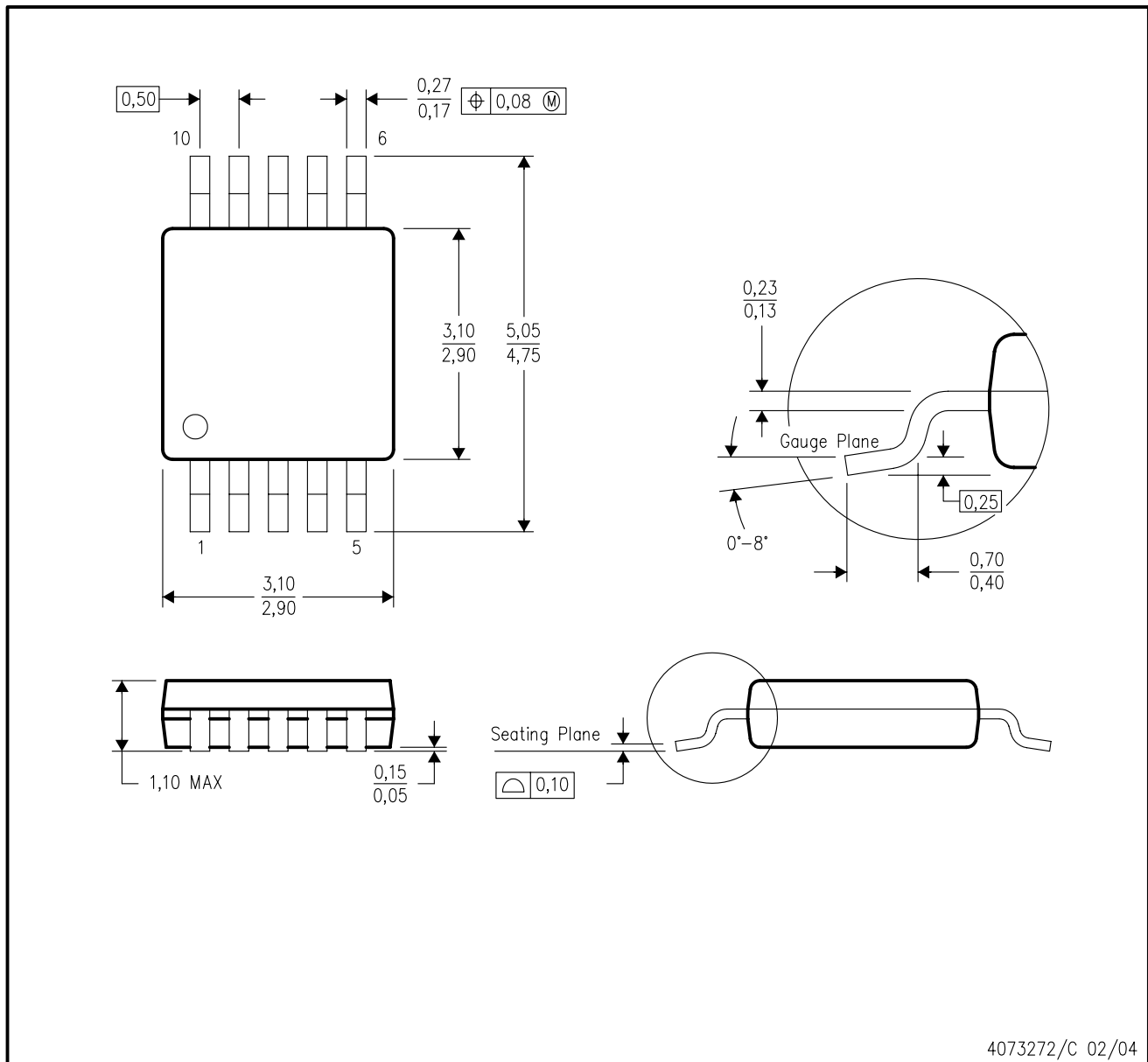
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5030MM	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM5030MM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM5030MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LM5030SD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



4073272/C 02/04

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation BA.

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